

Abstract of the Disclosure:

An electronic component has a chip stack with a first semiconductor chip, a second semiconductor chip, and a large number of flat conductors configured in between the first  
5 semiconductor chip and the a second semiconductor chip. The flat conductors have a central section on which the semiconductor chips are mounted. First bonding connections connect the first semiconductor chip to inner sections of the flat conductors. Second bonding connections connect the second  
10 semiconductor chip to transitional sections of the flat conductors. The outer sections of the flat conductors project out of a package.

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